Single-Gate MESFET Frequency Doublers

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Abstract—**A simple analytic model of the FET frequency doubler is used to determine the relative contributions of the various nonlinearities to harmonic generation. FET doubler conversion gain and its variation with frequency relative to the fundamental frequency available gain is also estimated. Large-signal computer simulations are used to determine the validity of the analytic model and provide further information on conversion gain and its frequency dependence. The analytic and computer predictions are compared with experimental measurements on a 4- to 8-GHz single-gate FET frequency doubler.**

I. Introduction

GaAs MESFET'S operated as frequency multipliers are attractive because they provide conversion gain over a broad frequency band and also have some isolation between the input and output ports. In the GaAs monolithic integrated circuit context, the fabrication of FET multipliers is preferable to the processing of p-n junction varactor or Schottky-diode multipliers in the presence of other FET circuits. Hence, there is considerable interest in FET harmonic generators at the present time.

Experimental results on both single- and dual-gate FET frequency multipliers have been published [1]–[5] and limited results are available from a computer simulation of a single-gate FET multiplier [4]. The object of the present paper is to determine the relationship between the conversion gain of the single-gate FET frequency doubler and the fundamental frequency gain of the device and also predict its frequency limitations.

Simple analytic considerations of the single-gate FET determine the relative contributions of the various nonlinearities to harmonic generation. Based on these, the FET frequency doubler conversion gain and its frequency variation is related to the device fundamental frequency gain. Computer simulations, initially using a unilateral model and subsequently a more complex but realistic model, examine the validity of these results. Experimental measurements on a 4–8-GHz doubler using a commercial medium power *C*-band FET (MSC88001) are compared with simulation results to determine the accuracy of the large-signal computer model.

II. Theoretical Considerations

The equivalent circuit in Fig. 1 is considered as representative of a common-source medium-power single-gate FET. The parameter values of the circuit elements in this figure title are those of a commercial medium power *C*-band FET (MSC 88001), estimated from small-signal scattering parameter measurements. The $I_{ds}-V_{ds}$ characteristics of this device related to this model are given in Fig. 2. Note that the curves are an approximation to the measured characteristics of this device in that the output conductance always remains positive. The use of these characteristics makes the calculations quasi-static. The parameters for these curves give a pinchoff voltage V_p of -6 V, and an I_{ds} of 180 mA for 0-V gate bias and V_{ds} of 5 V. The straight line portions of these characteristics are given by

$$I_{ds} = I_{dss}\left(1-\frac{V_{gs}}{V_p}\right)^2\left(1+\frac{V_{ds}}{R_{do}I_{dss}}\right) \quad (1)$$

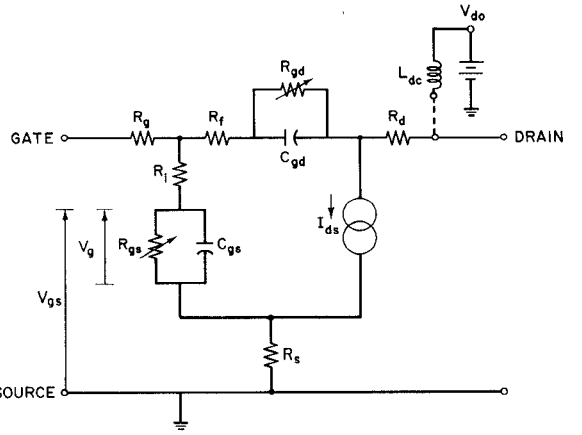

Fig. 1. Equivalent circuit for the MSC 88001 FET in the grounded source configuration. For the transistor used in the simulations the parameters are $R_g = R_d = 0\ \Omega$, $R_i = 26\ \Omega$, $R_f = 28\ \Omega$, $R_s = 1\ \Omega$, $C_{gs0} = 0.47$ pF, $C_{gd0} = 0.25$ pF. Note that the bias circuit is removed when the device is used with the load circuit of Fig. 3(b)

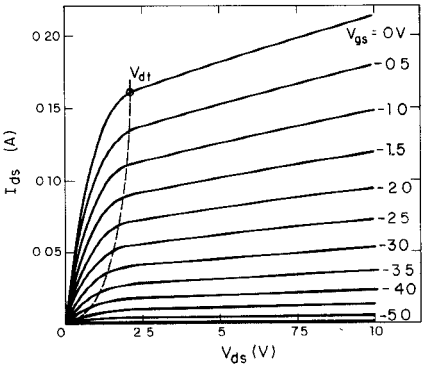

Fig. 2. $I_{ds}-V_{ds}$ characteristics for the device in Fig. 1.

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where I_{dss} is the drain–source saturation current; V_{ds} is the drain–source voltage; V_{gs} is the gate–source terminal voltage; R_{do} is the output conductance; and V_p is the gate pinchoff voltage. The curved sections of the characteristics are cubics, chosen to become tangential to the above straight lines along a parabola which passes through the origin and intersects the 0-V bias line at V_{dt} as shown in Fig. 2. The full expression for these characteristics is given in the Appendix. The simplified model calculations use (1) as the $V_{gs}-I_{ds}$ transfer characteristic with R_{do} assumed to be large.

The major nonlinearities in the FET causing harmonic generation are: 1) the gate–source and gate–drain nonlinear capacitors C_{gs} and C_{gd}, which represent the gate–junction depletion layer capacitance [6]; 2) the drain current I_{ds} nonlinearity, which arises when the current is clipped when V_{gs} swings below pinchoff and/or swings positive to cause the gate diode, represented by R_{gs}, to conduct; 3) the nonlinearity of the $V_{gs}-I_{ds}$ transfer characteristic, which in the present instance is assumed to be quadratic, as given by (1) and (A.1), but in practice is more complex; and 4) the output conductance nonlinearity. The contributions of each of these are included in the calculations.

III. Simplified Analysis

The calculations in this section omit the gate–drain branch of the equivalent circuit (see Fig. 1), and assume that $R_s = 0$, that the load is resistive and that the $V_{gs}-I_{ds}$ transfer characteristic is given by (1), unless specified otherwise, and holds over the whole positive $I_{ds}-V_{ds}$ quadrant. Omission of the gate–drain branch is an acceptable approximation since the capacitance C_{gd} becomes small over the relevant range of biasing conditions.

A. Effect of Gate–Source Capacitor

The input capacitor C_{gs} and series resistance R_i, of the gate–source junction can be analyzed as a lossy varactor diode. The FET gate–source capacitance at 0-V bias is $C_{gs0} = 0.47$ pF, and the series resistance $R_i = 26\ \Omega$, and therefore the zero bias cutoff frequency of the diode is about 13 GHz. The second harmonic voltage generated across the capacitor from voltage-driven elastance calculations [7], [8] is approximately 12–30 percent of the fundamental, depending on the value of breakdown voltage chosen. In the absence of other nonlinearities, this result suggests that the second harmonic level due to the nonlinearity is of the order of -18 to -11 dB relative to the fundamental.

B. Effect of I_{ds} Clipping Nonlinearity

When the FET is biased close to 0 V, just below the forward conduction point of the gate–source junction, the voltage waveform across the gate–source capacitor is clipped due to junction conduction. The waveform takes the half-wave rectified form, assuming that the negative maximum does not reach pinchoff, and is transferred to I_{ds} through the transfer characteristic. Fourier analysis of the half-wave rectified form gives a fundamental voltage component magnitude of $V/2$ and a second harmonic voltage magnitude of $(2V/3\pi)$. Neglecting the transfer characteristic nonlinearity, the second harmonic output power level is 7.4 dB below the fundamental component.

When the device is biased at the pinchoff voltage, the drive voltage causes the FET to be turned on only during the positive half-cycles of the drive waveform. The output waveform would again take the near half-wave rectified form, assuming that the gate voltage did not rise to the forward conduction point. Neglecting the nonlinear transfer characteristic, a similar value of second harmonic level would be obtained. In a practical FET, the transfer characteristic is nonlinear, and the transconductance g_m falls off as pinchoff is approached. However, since the average value of C_{gs} becomes lower at the more negative bias, this fall in g_m may be offset by the increase in voltage swing across C_{gs}, causing an increase in gain [5].

C. Effect of $V_{gs}-I_{ds}$ Transfer Characteristics and Output Conductance

The transfer characteristic in (1) may be simplified to

$$I_{ds} = I_{dss}\left(1-\frac{V_{gs}}{V_p}\right)^2 f(V_{ds}, R_{do}). \tag{2}$$

For the present, $f(V_{ds}, R_{do})$ is assumed to be constant. A sinusoidal excitation for V_{gs} of the form $(V_0 + V_1 \sin \omega t)$ gives rise to the following terms (assuming no clipping occurs):

$$I_{ds} = I_{dss}\left[\left\{\left(1+\frac{V_0}{V_p}\right)^2 + \frac{V_1^2}{2V_p^2}\right\} - 2\left(1-\frac{V_0}{V_p}\right)\frac{V_1}{V_p}\sin\omega t - \frac{V_1^2}{2V_p^2}\cos 2\omega t\right]. \tag{3}$$

The ratio of the second harmonic to fundamental current magnitudes at the current generator is given by

$$\left|\frac{I_{2f}}{I_f}\right| = \left|\frac{V_1}{4V_p\left(1-\frac{V_0}{V_p}\right)}\right|. \tag{4}$$

For $V_p = -6$ V, the gate biased at midpoint, so that $V_0 = -3$ V and $V_1 = 3$ V, this ratio becomes 1/4. Therefore, the second harmonic level due to this nonlinearity is approximately 12 dB below the fundamental.

Inclusion of the output conductance nonlinearity is effected by allowing the term $f(V_{ds}, R_{do})$ in (2) to vary. Suppose the load circuit comprises a resistance, R_l, in shunt with a RF choke, fed from a drain supply of voltage V_{d0}, giving rise to an average current of I_{d0} (see Fig. 3(b)). Then

$$V_{ds} = V_{d0} - (I_{ds} - I_{d0})R_l. \tag{5}$$

Assuming a sinusoidal excitation for V_{gs} for the form $(V_0 + V_1 \sin \omega t)$, as above, and substituting in (1) and (5)

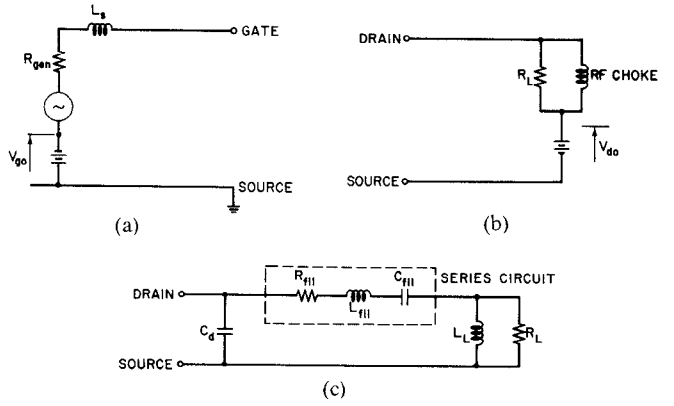

Fig. 3. Input and output circuits for FET. (a) Input circuit (b) Resistive load circuit. (c) Tuned load circuit. Series circuit is resonant at $2f$ and C_d and L_l are parallel resonant at $2f$ for doubler operation. Note the new drain bias circuit with resistive load in (b).

gives

$$I_{ds}=\frac{\left(1-\dfrac{V_0+V_1\sin\omega t}{V_p}\right)^2\left(\dfrac{V_{d0}+I_{d0}R_l}{R_{do}}+I_{dss}\right)}{1+\left(1-\dfrac{V_0+V_1\sin\omega t}{V_p}\right)^2\dfrac{R_l}{R_{do}}}. \quad (6)$$

Simplifying this for a wide range of parameters is difficult. For $R_l \ll R_{do}$, the results of (4) are approximately valid, but for other values of R_l the level of the second harmonic component relative to the fundamental has to be estimated numerically.

When the bias point approaches pinchoff or gate forward conduction, the waveform in the above expression (6) for $V_1 \sin\omega t$ has to be modified to include the clipping effect. The simplification of the expression derived from (6) also becomes difficult, and therefore the analysis is computed as described in Section IV.

D. Results of Analysis

Based on the above discussions, the FET doubler has a peak in conversion gain (or minimum conversion loss) with the gate biased close to 0 V or pinchoff, and this would be about 6 to 8 dB below the corresponding fundamental frequency gain. At gate bias midway between these extremes, the conversion gain is expected to drop a further 4–6 dB relative to the fundamental gain. These figures will be modified somewhat at high drive levels.

In the absence of transit time effects, the fundamental frequency gain of the device falls at 6-dB octave, and the second harmonic gain, which is about 6–8 dB less than the fundamental gain, also falls at the same rate. This suggests that second harmonic conversion becomes lossy as the doubler output frequency approaches the device small-signal unity-gain frequency f_T.

IV. Computer Large Signal Modeling

The nonlinear behavior of the FET cannot be easily characterized, as seen above, and therefore computer modeling is the only means of completely analyzing the FET doubler. The modeling predicts FET doubler performance and also determines the validity of the simple analytic results in Section III.

The large-signal model in the present simulation uses the FET equivalent circuit shown in Fig. 1, and input and load circuits as in Fig. 3. The transfer characteristics for the particular load circuit trajectory are determined from the $I_{ds}-V_{ds}$ characteristics in Fig. 2 for known values of V_{gs} and V_{ds}. The circuit model together with its characteristics are analyzed in the time domain by integration of appropriate differential equations.

The equivalent circuit model represents the gate depletion-layer as two nonlinear capacitors each shunted by nonlinear resistors. The variation of the gate–source capacitor with voltage is given by

$$C_{gs}=C_{gs0}\left(1-\frac{V_g}{V_{bi}}\right)^{-1/2} \quad (7)$$

where C_{gs0} is the gate–source capacitance at 0-V gate bias; V_g is the voltage across the capacitor; and V_{bi} is the built-in gate–source junction voltage. The nonlinear resistor R_{gs} represents the gate–source junction, and the conduction current through it is given by

$$I_{gs}=I_{gs0}(\exp\alpha V_g-1) \quad (8)$$

where I_{gs0} is the leakage current through the junction $\alpha=q/nKT$, where n is the ideality factor of the junction, equal to unity in these calculations.

Similarly, C_{gd} and R_{gd} represent the gate–drain junction and their values are determined from equations similar to (7) and (8), with the gate–drain voltage V_{gd} as the independent variable. The output conductance at the current generator is included in the characteristics in Fig. 2 and (A.1) and therefore is not specified in the output circuit. The bias circuit is omitted from Fig. 1 when the resistive load circuit in Fig. 3(b) is used. Package and device parasitics have been omitted, with the exception of C_d in Fig. 3(c), because they increase the complexity of the simulation and do not contribute to the physical mechanisms of harmonic generation.

Time-derivative differential equations for currents and voltages are set up for the appropriate model including the input and load circuits, and integrated using the Gear [9] routine. The current generator I_{ds} is determined from the values of V_{ds} and V_{gs} in (A.1). Note that V_{gs} includes the voltage across C_{gs} and R_s, since the characteristics in Fig. 2 are derived from the static characteristics which retain this drop. Omission of the R_s drop from V_{gs} only changes the results by a few percent.

The gate transit time τ varies with V_{gs}, but for simplicity may be approximated by a constant value which is the gate length divided by the saturated velocity ($\sim 10^7$ cm/s). In the time domain its effect is accounted for by averaging the value of V_{gs} over the past time period τ when estimating the drain current I_{ds}. However, for the present simulations, the transit time effect was omitted as it was thought that the computational time would increase considerably. The transit time effect becomes important as input and output

frequencies approach $f_t = 1/\tau$; however, the frequency f_t is much higher than those considered here.

The simulations use two models, a simple unilateral FET with a resistive load model, in which the various nonlinearities are introduced in sequence, and the complete model, which uses a tuned load circuit. Input current and voltage waveforms and similar output waveforms across the load resistor are Fourier analyzed to estimate the dc, fundamental, and harmonic components.

A. Unilateral Model

This model omits the gate–drain branch, which makes the device unilateral, and also omits the source resistance R_s. It is assumed that the input circuit (as in Fig. 3(a)) comprises the RF source, the gate-bias source, the generator resistance which matches the gate resistance, and a series inductor which matches the gate–source capacitor. The load circuit, as in Fig. 3(b), is a resistive load shunted by a large inductor (which is a short circuit at dc and an open circuit at RF), and the drain bias is connected through this circuit.

Simulations were performed in four cases, with increasing numbers of nonlinearities. Each case assumes that I_{ds} clipping occurs and also that C_{gs} is constant, determined by the dc gate bias as per (7), with a perfect diode across it, except in case (*iv*). These simulations are: (*i*) with $V_{gs}-I_{ds}$ linear characteristics; (*ii*) with the $V_{gs}-I_{ds}$ quadratic form as in 2(b), with $f(V_{ds}, R_{d0})$ set to unity; (*iii*) with the characteristics including the output conductance variation as in (A.1); and (*iv*) with C_{gs} varying as per (7), with gate–source junction current given by (8), characteristics as in (*iii*).

The parameters used in these computations are summarized in Table I. Fig. 4(a) and (b) show typical results of the variation of doubler gain against V_{gs} for an input frequency of 4 GHz with this model. Fig. 4(a) illustrates doubler behavior at a low input power (6.8 dBm). All curves here show that the conversion gain peaks near 0-V gate bias and near pinchoff as predicted in Section III. The midpoint bias minimum doubler gain position is present in all curves, but their position varies with the nonlinearities included. The minimum is about 15 dB below the doubler gain peak in case (*iv*) above and even lower in the other cases. The linear characteristic case (*i*) shows a second minimum as a consequence of the increase in C_{gs} with bias reducing the effect of I_{ds} clipping.

The overall doubler gain curve shape changes from the linear characteristic case (*i*), when the quadratic characteristics in (*ii*) are used. There is little change in the results when the output conductance variation is also included in (*iii*). Inclusion of the C_{gs} variation with V_{gs}, and the gate–source junction current, in (*iv*) changes the curve shape by reducing the negative value at the minimum and by moving its position towards pinchoff. The variation of C_{gs} with V_{gs} also increases the peak gain by 1 or 2 dB, confirming that the contribution of this nonlinearity is small. Thus, the I_{ds} clipping nonlinearity is the major contributor to harmonic generation, with additional contributions from the transfer nonlinearity and the C_{gs} nonlinearity. The peak of the doubler gain, however, is about 10 dB below the corresponding fundamental frequency gain close to 0-V bias and pinchoff, and the minimum in case (*iv*) is almost 22 dB below the corresponding fundamental frequency gain.

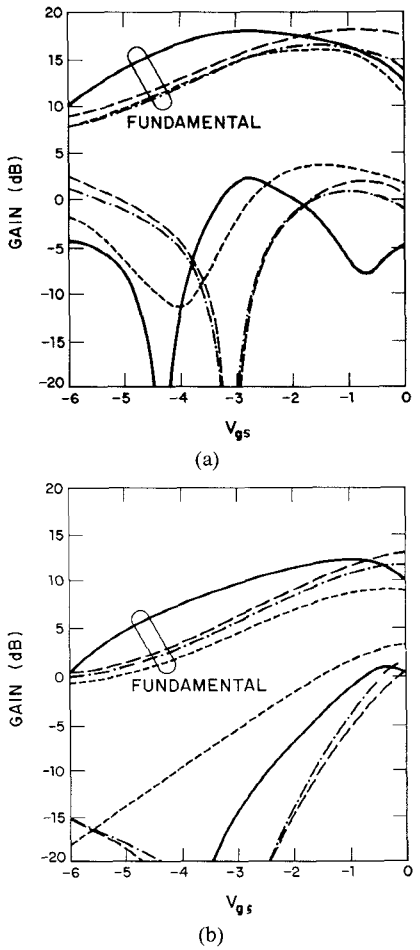

Fig. 4. Simulation results for a 4- to 8-GHz FET doubler as a unilateral device with (a) 6.8-dBm input and (b) 16.4-dBm input power. $V_{ds} = 5$ V. (*i*)——— linear $V_{gs}-I_{ds}$. (*ii*)— — —quadratic $V_{gs}-I_{ds}$. (*iii*)— · — · — $I_{ds}-V_{ds}$ characteristics. (*iv*)----C_{gs} varies with instantaneous gate voltage.

The results in Fig. 4(b) are at the higher input drive of 16.4 dBm at 4 GHz, and the patterns show considerable differences from Fig. 4(a). The linear characteristic case (*i*) shows large doubler conversion loss when biased near pinchoff, because the small value of C_{gs} causes the drain current waveform to become near square wave in form as a result of clipping due to both pinchoff and gate conduction. As the gate bias is increased towards 0 V, the waveform becomes asymmetric leading to an increase the second harmonic content. The curve shapes with the quadratic characteristics in (*ii*) and output conductance in (*iii*) are similar, except that the quadratic nonlinearity increases the second harmonic near pinchoff. The minimum gain in these cases is higher than the linear characteristics case (*i*). The effect of output conductance nonlinearity is again seen to be small.

When the C_{gs} variation with drive is included, the peak

TABLE I
THE PARAMETERS USED IN THE FOUR CASES OF THE UNILATERAL MODEL SIMULATION; V_{gs0} IS THE DC BIAS OF THE GATE

Case No.	I_{ds} Relationship	C_{gs} Variation	Gate-Source Junction Current
(i)	constant x V_{gs}	$C_{gso}\left(1-\frac{V_{gso}}{V_{bi}}\right)^{-1/2}$	0
(ii)	$I_{dss}\left(1-\frac{V_{gs}}{V_p}\right)^2$	$C_{gso}\left(1-\frac{V_{gso}}{V_{bi}}\right)^{-1/2}$	0
(iii)	$I_{dss}\left(1-\frac{V_{gs}}{V_p}\right)^2\left(1+\frac{V_{ds}}{R_{do}I_{dss}}\right)$ and associated cubics as in Eq. (A.1).	$C_{gso}\left(1-\frac{V_{gso}}{V_{bi}}\right)^{-1/2}$	0
(iv)	$I_{dss}\left(1-\frac{V_{gs}}{V_p}\right)^2\left(1+\frac{V_{ds}}{R_{do}I_{dss}}\right)$ and associated cubics as in Eq. (A.1)	$C_{gso}\left(1-\frac{V_{gs}}{V_{bi}}\right)^{-1/2}$	$I_{gso}(e^{\alpha V_g}-1)$

value of doubler gain near 0-V bias increases by about 2 dB, increasing to this value monotonically from minimum gain at pinchoff. In this case, the increased drive causes the waveform to become near square wave at biases near pinchoff, with increasing asymmetry as bias is moved towards 0 V. This appears to be the cause of the doubler gain curve shape seen in this Fig. 4(b) for case (*iv*).

Note that with large drive, the highest doubler gain occurs near 0-V bias and is about 6 dB below the corresponding fundamental frequency gain, as predicted earlier.

B. Full Model Simulation

This simulation uses the full equivalent circuit in Fig. 1, including the gate–drain series resistance and capacitor with its shunt diode, and the source series resistance R_s. The model is more representative of practical FET's; it allows negative excursions of the drain voltage by postulating similar characteristics as in Fig. 2 in the negative I_{ds} and V_{ds} third quadrant with V_{gd} as the controlling voltage. Breakdown at the junctions has not been included in the model and therefore predictions of device power handling capability are optimistic.

Selection of the value of C_{gd} is difficult. The results of Willing, Rauscher, and deSantis [6] suggest that C_{gd} does not fall according to the conventional abrupt junction variation with voltage given by

$$C_{gd}=C_{gd0}\left(1-\frac{V_{gd}}{V_{bi}}\right)^{-1/2} \tag{9}$$

Other authors [10] suggest that C_{gd} is purely parasitic and that any variation with voltage V_{gd} can be neglected. It would seem that this capacitor is a combination of the parasitic and part of the gate depletion layer capacitance, with the latter becoming small because of the drain bias. The variation of this part of the depletion layer capacitance would logically seem to follow the form in (9) above, with the inclusion of a factor to account for the geometric effect. However, the value of C_{gd0} for the present case was taken to be lower than the value of C_{gs0} without any geometric factor, and the parasitic capacitance was not included. The value chosen for C_{gd0} for these particular simulations is about half C_{gs0}, since this allows the C_{gd} variation to approach that predicted by Willing *et al.* [6]. The variation of the C_{gd} with voltage also contributes to the device nonlinearity, but in general this is not a significant factor in harmonic generation because of the large negative bias across it, and large value of associated series resistor.

Some results of the computation for a 4- to 8-GHz doubler, are given in Fig. 5, which is a plot of doubler conversion gain against gate-bias voltage for two different values of input power. Results at lower input powers have been omitted for clarity, since these follow similar trends. Included in this figure are the experimental results for a 4- to 8-GHz doubler, which are discussed below. Note the good agreement between the simulation and experiment. Fig. 6 shows both fundamental gain and doubler conversion gain as a function of RF input power, for different input frequencies at 0-V gate bias. The fundamental gain falls at 6 dB/octave at low input power, and the doubler gain also falls in a similar fashion, but is input-power dependent. Note that doubler conversion gain is negative at input frequencies above 4 GHz.

The full simulation has been performed with a specific circuit topology and circuit parameters. The results show

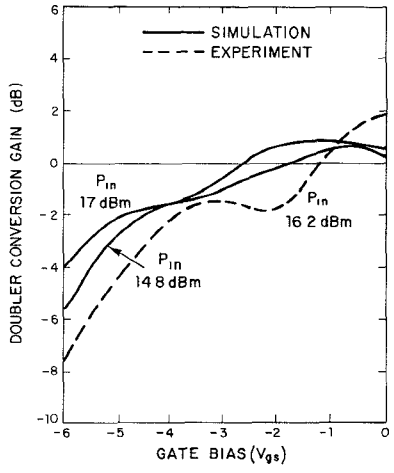

Fig. 5 Simulation results for a 4- to 8-GHz FET doubler using the full equivalent circuit model for input powers of 14.8 dBm and 17 dBm. Experimental results on the MSC 88001 device for an input power of 16.2 dBm is also shown for $V_{ds} = 5$ V, $V_{gs} = 0$ V.

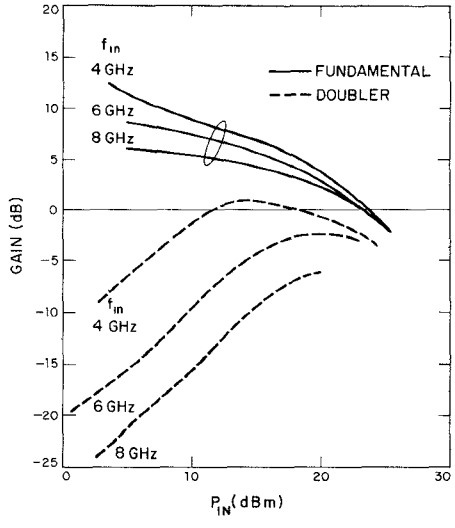

Fig. 6. Simulation results showing fundamental and doubler gain for the FET doubler using the full equivalent circuit for input frequencies of 4, 6, and 8 GHz, as a function of input power, for $V_{ds} = 5$ V and $V_{gs} = 0$ V.

some variation in detail from the analytic results of Section III and the resistive load unilateral results in Fig. 4, but are in good overall agreement.

V. Experimental Results

Experiments were performed on a commercial *C*-band, medium power packaged FET (MSC 88001), not specifically designed for doubler operation, in a 4- to 8-GHz doubler circuit. The device is mounted in a microstrip jig between two triple slug tuners and adjacent bias-T's. Couplers with power meters measure the input incident, reflected, and output powers. Input low-pass and output high-pass filters were also included in the test circuit. The output frequencies were monitored by means of a spectrum analyzer which also provided an approximate measure of the output power.

The package parasitics in this device cause the gate and drain ports to become series resonant at around 6 GHz. Thus, comparisons of the experimental results with theory are at best approximate. The experimental results are also taken with the circuit retuned for every input power level and gate bias change, and this is in contrast to simulation results which have fixed input and output circuits for any particular frequency. Results of experiments with fixed circuits show similar behavior to and good agreement with the simulation results of Fig. 5. At maximum doubler gain, the power-added efficiency was 8.2 percent.

Experimental results at higher frequencies show large conversion loss similar to those in Fig. 6, and have therefore not been included.

Conclusions

A simple analytic model has been used to estimate the contribution of the FET nonlinearities to doubler operation. The magnitude of doubler conversion gain and its frequency variation relative to the FET fundamental frequency gain are also estimated. Large signal computer simulations determine the limitations of the analytic model, and also provide a wider range of results. Experimental measurements on a 4- to 8-GHz doubler using a commercial FET show good agreement with theoretical predictions and simulation results.

This paper has shown that the largest contributor to the FET frequency doubler operation is the I_{ds} clipping effect. This suggests that the device is principally a resistive doubler and therefore harmonic conversion gain is expected to fall as $(1/n)^2$, where n is harmonic number.

Appendix

The characteristics of the FET in Fig. 2 are given by

$$I_{ds} = \left(1 - \frac{V_{gs}}{V_p}\right)^2 \left(I_{dss} + \frac{V_{ds}}{R_{do}}\right), \qquad \text{for } V_{ds} > V_{\tan}$$

$$= \left(1 - \frac{V_{gs}}{V_p}\right)^2 \left\{I_{dss} + \frac{V_{ds}}{R_{do}} - I_{dss}\left(\frac{V_{\tan} - V_{ds}}{V_{\tan}}\right)^3\right\}, \qquad \text{for } V_{ds} < V_{\tan}. \quad \text{(A.1)}$$

$V_{\tan}$ lies on the parabola passing through the origin, and the point (V_{dt}, I_{dt}), where

$$I_{dt} = \left(I_{dss} + \frac{V_{dt}}{R_{do}}\right). \quad \text{(A.2)}$$

It follows that

$$V_{\tan} = V_{00}\left\{1 + \left(1 + \frac{2R_{do}I_{dss}}{V_{00}}\right)^{0.5}\right\} \quad \text{(A.3)}$$

where

$$V_{00} = \frac{\left(1 - \frac{V_{gs}}{V_p}\right)^2 V_{dt}^2}{2(I_{dss}R_{do} + V_{dt})}. \quad \text{(A.4)}$$

In the practical FET $V_{dt} \leq |V_p/2|$. From small signal *S*-parameter measurements R_{do} at $V_{gs} = 0$ V is determined,

and from this I_{dss} may be obtained from the value of I_{ds} at 0-V bias.

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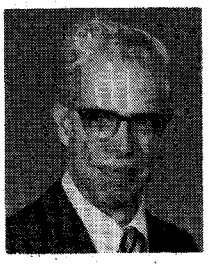

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p-i-n Diodes for Low-Frequency High-Power Switching Applications

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Abstract—**The development of high-power low-frequency diodes, conditions for their operation, and results measured in actual circuits are described. Harmonic distortion at 500 kHz and 2 MHz has been found to decrease with increasing diode lifetime and forward-bias current. Large reverse bias voltages are necessary at low frequencies to keep the RF voltage swing from penetrating the forward conduction region. The improvement of p-i-n diode lifetimes with thicker I-layers or with planar construction has been studied and the performance of these diodes in a routing switch is reported.**

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I. INTRODUCTION

WITH the successful design and fabrication of p-i-n diodes for high-voltage switches at microwave frequencies [1], their application at lower frequencies can now be investigated. This paper stems from the successful effort

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